What is claimed is:

1. A test method comprising:

a) obtaining test measurement values on a device at a plurality of independent variable values;

b) calculating the goodness of fit value for a fitted curve between :

(1) said test measurement values; and

(2) the independent variable values;

c) using said goodness of fit value to monitor the processes used to form said device.

2. The method of claim 1 wherein step (c) further includes using control limits on the goodness of fit values.

3. The method of claim 1 wherein step (c) further includes using control limits on the goodness of fit values; said control limits established based on a history of goodness of fit values or on device requirements.

4. The method of claim 1 wherein the goodness of fit is a correlation coefficient or a standard error measurement.

5. The method of claim 1 wherein the fitted curve is a least squares fitted straight line.

6. The method of claim 1 wherein the test measurement values are resistance or capacitance measurements values.

7. A test method comprising:

a) providing a device structure that has at least a first test structure, a second test structure and a third test structure incorporating a resistive portion from which resistance is measured;

(1) said resistive portion having an effective length (Lx) and an effective width (Wx),

(2) said first, second and third test structures have resistive portions with different effective widths (W1 W2, ... Wi);

(3) said resistive portion of said first, second and third type test structures have effective lengths (L1, L2, .. Li);

b) measuring the resistance (R) of the test structures;

c) calculating the goodness of fit value for a fitted curve between:

(1) said effective length divided by the measured resistance (L1/R1, L2/R2, ..Li /Ri); and

(2) the effective widths (W1, W2, ..Wi) of the test structures;

d) using said goodness of fit value to: (1) control the processes used to form the device or (2) screen the devices.

8. The method of claim 7 wherein said fitted curve is a fitted straight line fitted using a least squares method.

9. The method of claim 7 wherein said test structures are formed in and/or over a wafer.

10. The method of claim 7 wherein said test structures are comprised of a doped region in a wafer.

11. The method of claim 7 wherein said test structures are comprised of a material that has a measurable resistance.

12. The method of claim 7 wherein said test structures are comprised of a conductive material and an interconnect layer in a semiconductor device is comprised of said conductive material.

13. The method of claim 7 wherein said test structures are comprised of metal from a metal layer that is used to form metal lines in a semiconductor device.

14. The method of claim 7 wherein said test structures are comprised of a material selected from the group consisting of silicon, amorphous silicon, polysilicon, polycide, silicide, metal, copper, aluminum, and alloys and combinations thereof.

15. The method of claim 7 wherein said goodness of fit value is a correlation coefficient, coefficient of determination or standard error measurement test.

16. The method of claim 7 wherein said resistive portions have said effective length being substantially greater than said effective width and said effective width being selected to be substantially greater than an expected critical dimension loss for said process.

17. The method of claim 7 wherein the measuring the resistance (R) of the test structures; comprises measuring the resistance at different temperatures; and
further includes : calculating the goodness of fit value for a straight line for the between :
(1) the effective length divided by the measured resistance (L1/R1, L2/R2, ..Li /Ri).; the effective length of the test structure are equal (L1 = L2 =.. Li) and
(2) the effective widths (W1, W2, ..Wi) of the test structures; and
(3) the temperature.

18. The method of claim 7 wherein said device structure is a wafer; said wafer has at least three test structures;
the goodness of fit measurement is calculated on measurements made on the test sites on said wafer.

19. The method of claim 7 wherein said device is a printed circuit board, a ceramic substrate or a chip scale package.

20. The method of claim 7 wherein structures are formed adjacent to said resistive portion to measure the effects of micro loading or chemical-mechanical polishing,

21. A method for estimating defect levels by goodness of fit measurements related to resistance of an interconnect layer in a process for manufacturing an integrated circuit, said method comprising the steps of:

a) fabricating on a wafer, using said manufacturing process at least a first test structure, a second test structure and a third type test structure incorporating a resistive portion from which a resistance is measured,

b) said resistive portion having an effective length and an effective width, said effective length being substantially greater than said effective width and said effective width being selected to be substantially greater than an expected critical dimension loss for said process;

c) measuring said resistance; and

d) deriving the sheet resistance from the resistance measurement;

e) calculating a goodness of fit value between the one divided by the sheet resistance (1/Rs) and a second parameter;

f) using said goodness of fit value to: (1) control the processes used to form the test structures or (2) screen the test structures.

22. The method of claim 21 where said second parameter is the effective width of the test structures or the temperature.

23. A test method comprising:

a) providing a device structure that has at least a first test structure, a second test structure and a third test structure from which a test parameter is measured;

b) measuring the test parameter values on the test structures;

c) calculating the goodness of fit value for a fitted curve between :

(1) the test parameter values and

(2) a dimensional measurement of the test structures;

d) using said goodness of fit value (of the L/R vs W) to: (1) control the processes used to form the device structures or (2) screen the device structures.

24. The method of claim 23 wherein said test parameter is resistance or capacitance.

25. A test method comprising:

a) providing a device structure that has at least a first test structure, a test measurement can be obtained from said first test structure;

b) measuring a first test measurement of the test structures;

c) calculating the goodness of fit value for a fitted curve between :

(1) a first test measurement performed under a first test condition and

(2) a second test measurement performed under a second test condition;

d) using said goodness of fit measurement to: (1) control the processes used to form the device or (2) screen the devices.

26. The method of claim 25 wherein: said first test condition and said second test condition are different temperatures.

27. The method of claim 25 wherein:

said first test structure is a resistance test structure that has a effective length (L) and effective Width (W);

said first and said second test conditions have different temperatures;

said first test measurement is a resistance test measurement;

said goodness of fit measurement is for a straight line fitted to (1) the effective length (L) divided by the resistance (R) vs (2) the effective width (W).